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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/651,385	08/29/2000	Sanjay Dabral	042390.P5258D	9681

7590 02/11/2004

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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,385	DABRAL ET AL.	
	Examiner	Art Unit	
	José R Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-23 and 26-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-23 and 26-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to an amendment filed December 4, 2003 on which Applicant amended claim 20 to incorporate the limitations of claims 24 and 25, as instructed by the examiner in the Office action mailed on November 6, 2003. However, upon even further consideration claims cannot be allowed in view of Ker et al. (US Pat. No. 5,714,784). Any inconvenience to applicant is sincerely regretted.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 20-23 and 26-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Ker et al. (US Pat. No. 5,714,784).

Regarding claim 20, Ker et al. teaches a method of forming an integrated circuit comprising: forming a performance circuit (42) (see fig. 4) occupying a first well (i.e. twin well) of an integrated circuit substrate (see col. 4, lines 11-18); forming a protection circuit (45) (see fig. 4) occupying a second well (i.e. twin well) of the integrated circuit substrate (see col. 4, lines 11-18) separated from the first well (see fig. 4) wherein forming a protection circuit includes forming a unit diode (45), the unit diode (45)

comprised of a block of a doped region of the integrated circuit substrate occupying an area of the substrate sufficient to support a contact to the doped region (see fig. 4), a junction region (the surrounding region formed between the doped region N+ and the substrate) of the integrated circuit substrate surrounding the doped region (see fig. 2), and a contact (VDD) to the doped region (see fig. 2), the doped region being a first doped region of a first dopant (N+) (see fig. 2) in the second well (i.e. twin well) of the substrate (see fig. 4 and col. 4, lines 11-18), the second well (i.e. twin well) being doped with a first concentration of a second dopant (see col. 4, lines 11-18) and the junction region separating the first doped region from the second well (see fig. 4), wherein forming a protection circuit includes forming a third doped region (44) in the second well adjacent the junction region (see fig. 4), the third doped region (44) doped with a second concentration (P+) of the second dopant (see fig. 4); and coupling the protection circuit to the performance circuit (see figs. 2 and 4).

Regarding claim 21, Ker et al. teaches that the performance circuit includes a CMOS configuration (see col. 4, lines 14-15).

Regarding claims 22 and 23, Ker et al. teaches coupling the protection circuit or diode to a p-channel device of the CMOS configuration (see col. 4, lines 17-18).

Regarding claim 26, Ker et al. teaches forming a plurality of unit diodes (see region "S1" in figs. 2 and 4).

Regarding claim 27, Ker et al. teaches a method comprising: forming a performance circuit (42) (see fig. 4) occupying a first well (i.e. twin well) of an integrated circuit substrate (see col. 4, lines 11-18), wherein forming a performance circuit

includes: forming a unit transistor device (42) (see fig. 4) having a drain region (41) comprised of a doped region of the integrated circuit substrate occupying an area sufficient to support a contact to the doped region (see fig. 4); forming a gate region (42) of the integrated circuit substrate surrounding the doped region (41) (see fig. 4); and forming a contact (46) to the doped region (see fig. 4); forming a protection circuit (45) (see fig. 4) occupying a second well (i.e. twin well) of the integrated circuit substrate (see col. 4, lines 11-18) separated from the first well (see fig. 4); and coupling the protection circuit to the performance circuit (see figs. 2 and 4).

Regarding claim 28, Ker et al. teaches that the doped region (41) being a first doped region of a first dopant (N+) (see fig. 4) in a well of the substrate (see col. 4, lines 11-18), the well being doped with a concentration of a second dopant (see col. 4, lines 11-18) and wherein forming a performance circuit further comprises: forming a source region (43) of the transistor doped with the first dopant in the well separated from the drain region by the gate (42) to form a unit transistor (see fig. 4).

Regarding claim 29, Ker et al. teaches forming a plurality of unit transistor (42) (see fig. 4).

Response to Arguments

4. Applicant's arguments with respect to claims 20-23 and 26-29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lee et al. (US Pat. No. 6,097,066) discloses an ESD protection device wherein the gate (500) is surrounding the drain region (510) in figures 2 and 5.

Correspondence

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (703) 308-6078 or (571) 272-1727, after February 9, 2004. The examiner can normally be reached on 9:00-5:00 Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Tom Thomas
Supervisory Patent Examiner
Technology Center 2800

JRD